What Is Claimed Is:

1. A silicon wafer having a front surface, a back surface, a circumferential edge portion and a region between the front and back surfaces, the silicon wafer comprising:

a first denuded zone being formed up to a predetermined distance from the front surface;

a second denuded zone being formed up to a predetermined distance from the back surface; and

a bulk region being formed between the first and second denuded zones,

wherein a concentration profile of defects in the bulk region has a distribution which is maintained substantially constant in a direction from the front surface to the back surface.

2. A silicon wafer according to claim 1, wherein the defects are bulk micro-defects (BMD) including oxygen precipitates and bulk stacking faults.

3. A silicon wafer according to claim 2, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained constant in a range from about 3.0×10^{8} ea/cm^3 to about 1.0×10^{10} ea/cm^3.

4. A silicon wafer according to claim 1, wherein the defects are bulk stacking faults.

5. A silicon wafer according to claim 4, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained constant in a range from about 1.0×10^{8} ea/cm^3 to about 3.0×10^{9} ea/cm^3.

6. A silicon wafer according to claim 1, wherein the distances of the first and the second denuded zones from the front and back surfaces respectively are in a range from about 5 μm to about 40 μm.

7. A silicon wafer according to claim 1, wherein the first and the second denuded zones are substantially defectless regions in which oxygen precipitates and bulk stacking faults are substantially removed.

8. A silicon wafer having a front surface, a back surface, a circumferential edge portion and a region between the front and back surfaces, wherein the region between the front and back surfaces comprises:

a first denuded zone being formed up to a predetermined distance from the front surface;

a second denuded zone being formed up to a predetermined distance from the back surface; and

a bulk region being formed between the first and second denuded zones,

wherein a concentration profile of defects between the front and back surfaces of the wafer has a stepwise shape having an axial symmetry at the center between the front and back surfaces of the wafer,

wherein the bulk region has vertically-rising concentration gradients at boundaries of the first and second denuded zones and a horizontal concentration gradient over the bulk region, and

wherein a concentration profile of defects in the bulk region has a planar shape within a range of variation of about 10% or less.

9. A silicon wafer according to claim 8, wherein the defects are bulk micro-defects (BMD) including oxygen precipitates and bulk stacking faults.

10. A silicon wafer according to claim 9, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained constant in a range from about 3.0×10^8 ea/cm^3 to about 1.0×10^{10} ea/cm^3.

11. A silicon wafer according to claim 8, wherein the defects are bulk stacking faults.

12. A silicon wafer according to claim 11, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained constant in a range from about 1.0×10^8 ea/cm^3 to 3.0×10^9 ea/cm^3.

13. A silicon wafer according to claim 8, wherein the distances of the first and the second denuded zones from the front and back edges respectively are in a range from about 5 μm to about 40 μm.

14. A method of fabricating a silicon wafer comprising:

preparing a silicon wafer having a front surface, a back surface, a circumferential edge portion and a region between the front and back surfaces;

performing a first rapid thermal process to consume vacancies in the silicon wafer, thereby accelerating a formation of nuclei of oxygen precipitate; and

performing a second rapid thermal process to remove the nuclei of the oxygen precipitates located in a region near a front surface of the silicon wafer and to further accelerate the growth of the nuclei of the oxygen precipitates located in a bulk region of the silicon wafer.

15. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the second rapid thermal process is carried out at a higher temperature than that of the performing of the first thermal process.

16. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the first rapid thermal process is carried out at a temperature in a range from about 1120°C to about 1180°C.

17. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the second rapid thermal process is carried out at a temperature in a range from about 1200°C to about 1230°C.

18. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the first rapid thermal process is carried out for a time period in a range from about 1 second to about 5 seconds.

19. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the second rapid thermal process is carried out for a time period in a range from about 1 second to about 10 seconds.

20. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the first rapid thermal process utilizes an atmosphere of argon and ammonia.

21. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the first rapid thermal process and the step of performing the second rapid thermal process are carried out in-situ in the same apparatus.

22. A method of fabricating a silicon wafer according to claim 14, wherein the performing of the first rapid thermal process and the step of performing the second rapid thermal process are carried out ex-situ.

23. A method of fabricating a silicon wafer according to claim 14, wherein the preparing of the silicon wafer further comprises:

growing a silicon single crystal by immersing a seed crystal into a silicon melt and pulling the seed crystal while controlling a crystal growing rate and a temperature gradient in a growing direction at a crystal coagulation interface;

slicing the grown silicon single crystal into a shape of wafers; and

performing an etching process for removing slicing damages originated from the slicing step, and rounding a side surface of the sliced wafer or etching the surface.

24. A method of fabricating a silicon wafer according to claim 14, wherein the first and second thermal processes are carried out in a donor killing process for converting an oxygen which is generated in the silicon wafer at the time of the crystal growth into an oxygen precipitates in order to prevent the oxygen from emitting an electron in a subsequent thermal treatment process and functioning as a donor.

25. A method of fabricating a silicon wafer according to claim 14, wherein after performing of the second rapid thermal process, the method further comprises:

polishing the surface of the silicon wafer;

performing a mirror surface polishing process on the surface of the silicon wafer; and

cleaning the silicon wafer.

26. A method of fabricating a silicon wafer according to claim 14,

wherein after the performing of the first rapid thermal process and the step of performing the second rapid thermal process, the region between the front and back surfaces comprises:

a first denuded zone being formed up to a predetermined distance from the front surface;

a second denuded zone being formed up to a predetermined distance from the back surface; and

a bulk region being formed between the first and second denuded zones, and

wherein a concentration profile of defects in the bulk region has a distribution which is maintained substantially constant.

27. A method of fabricating a silicon wafer according to claim 26, wherein the defects are bulk micro-defects (BMD) including oxygen precipitates and bulk stacking faults.

28. A method of fabricating a silicon wafer according to claim 27, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained substantially constant in a range from about 3.0×10^{8} ea/cm^3 to about 1.0×10^{10} ea/cm^3.

29. A method of fabricating a silicon wafer according to claim 26, wherein the defects are bulk stacking faults.

30. A method of fabricating a silicon wafer according to claim 29, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained substantially constant in a range from about 1.0×10^{8} ea/cm^3 to 3.0×10^{9} ea/cm^3.

31. A method of fabricating a silicon wafer according to claim 26, wherein the first and the second denuded zones are disposed from the front and back surfaces respectively by distances in a range from about 5 μm to about 40 μm.

32. A method of fabricating a silicon wafer comprising:

(a) preparing a silicon wafer having a front surface, a back surface, a circumferential edge portion, and a region between the front and back surfaces;

(b) loading the silicon wafer in a rapid thermal processing apparatus;

(c) raising an internal temperature of the rapid thermal processing apparatus rapidly up to a first temperature of target;

(d) performing a first rapid thermal process at the first temperature for a time period which is needed to consume vacancies in the silicon wafer, thereby accelerating a formation of nuclei of oxygen precipitates;

(e) dropping the internal temperature of the rapid thermal processing apparatus rapidly down to a second temperature;

(f) raising the internal temperature of the rapid thermal processing apparatus rapidly up to a third temperature which is higher than the first temperature;

(g) performing a second rapid thermal process for maintaining the third temperature for a time period which is needed to remove the nuclei of the oxygen precipitates located in a region on a surface of the wafer or near the surface of the wafer and to further accelerate the growth of the nuclei of the oxygen precipitates located in the bulk regions of the silicon wafer; and

(h) dropping the internal temperature of the rapid thermal processing apparatus rapidly down to a fourth temperature.

33. A method of fabricating a silicon wafer according to claim 32, wherein the performing of the first rapid thermal process is carried out at a temperature in a range from about 1120°C to about 1180°C.

34. A method of fabricating a silicon wafer according to claim 32, wherein performing of the second rapid thermal process is carried out at a temperature in a range from about 1200°C to about 1230°C.

35. A method of fabricating a silicon wafer according to claim 32, wherein the performing of the first rapid thermal process is carried out for a time period in a range from about 1 second to about 5 seconds.

36. A method of fabricating a silicon wafer according to claim 32, wherein the performing of the second rapid thermal process is carried out for a time period in a range from about 1 second to about 10 seconds.

37. A method of fabricating a silicon wafer according to claim 32,

wherein during parts (b) to (h), argon gas is continuously supplied,

wherein during part (d), ammonia gas is supplied, and

wherein during parts (e) to (h), the supplying of the argon gas is blocked.

38. A method of fabricating a silicon wafer according to claim 32, wherein the preparing of the silicon wafer further comprises:

growing a silicon single crystal by immersing a seed crystal into a silicon melt and pulling the silicon single crystal while controlling a crystal growing rate and a temperature gradient of a growing direction at a crystal coagulation interface;

slicing the grown silicon single crystal into a wafer shape; and

performing an etching process for removing slicing damages originated from the slicing, and rounding a side surface of the sliced wafer or etching the surface.

39. A method of fabricating a silicon wafer according to claim 32, wherein parts (b) to (h) are carried out in a donor killing process for converting an oxygen which is generated in the silicon wafer at the time of the crystal growth into an oxygen precipitates in order to prevent the oxygen from emitting an electron in a subsequent thermal treatment process and functioning as a donor.

40. A method of fabricating a silicon wafer according to claim 32, wherein after part (h), the method further comprises of:

unloading the silicon wafer from the rapid thermal processing apparatus;

polishing the surface of the silicon wafer;

performing a mirror surface polishing process on the surface of the silicon wafer; and

cleaning the silicon wafer.

41. A method of fabricating a silicon wafer according to claim 32,

wherein after part (h), the region between the front and back surfaces comprises:

a first denuded zone being formed up to a predetermined distance from the front surface;

a second denuded zone being formed up to a predetermined distance from the back surface; and

a bulk region being formed between the first and second denuded zones, and

wherein a concentration profile of defects in the bulk region has a distribution which is maintained substantially constant.

42. A method of fabricating a silicon wafer according to claim 41, wherein the defects are bulk micro-defects (BMD) including oxygen precipitates and bulk stacking faults.

43. A method of fabricating a silicon wafer according to claim 42, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained substantially constant in a range from about 3.0×10^8 ea/cm^3 to about 1.0×10^{10} ea/cm^3.

44. A method of fabricating a silicon wafer according to claim 41, wherein the defects are bulk stacking faults.

45. A method of fabricating a silicon wafer according to claim 44, wherein the concentration of the defects in the region between the first and the second denuded zones has a distribution which is maintained substantially constant and in a range from about 1.0×10^8 ea/cm^3 to about 3.0×10^9 ea/cm^3.

46. A method of fabricating a silicon wafer according to claim 41, wherein the distances of the first and the second denuded zones from the front and back surfaces respectively are in a range from about 5 μm to about 40 μm.